TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED / ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371	ATTORNEY'S DOCKET NUMBER: P65633US0
	US APPLICATION NO (If known, see 37 CFR 1.5): 09/581185

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/IE98/00106	15 December 1998	15 December 1997

TITLE OF INVENTION

AN ATM CELL PROCESSOR

APPLICANT(S) FOR DO/EO/US

Kevin DEWAR, Brendan O'DOWD and Gavin BREBNER

Applicant herein submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information.

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for Internatl. Preliminary Examination was made by the 19th month from earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the Internatl. Preliminary Examination report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:

    International Search Report -EPO
    PCT Request Form
    PCT/IB/304 Form
    PCT/IB/308 Form
    First Page of Publication
    Demand
    International Preliminary Examination Report - with annexes

US APPLICATION NO.(If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/581185	PCT/IE98/00106	P65633US0

	CALCULATIONS	PTO USE ONLY
17. ☒ The following fees are submitted:		
Basic National Fee (37 CFR 1.492(a)(1)-(5)):		
Internatl. prelim. examination fee paid to USPTO (37 CFR 1.492 (a) (1)) . . $670.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.492 (a) (2)) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) . . $760.00		
Neither international preliminary examination fee (37 CFR 1.492 (a) (3)) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO) **$970.00**		
International preliminary examination fee paid to USPTO (37 CFR 1.492 (a) (4)) and all claims satisfied provisions of PCT Article 33(2)-(4) $96.00		
Search Report prepared by the EPO or JPO (37 CFR 1.492 (a) (5)) **$840.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 840.00	
Surcharge of $130.00 for furnishing the **oath or declaration** later than ☐ **20** ☒ **30** months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 130.00	

Claims	**Number Filed**	**Number Extra**	Rate		
Total Claims	**19** - 20 =	-0-	x $18.00	$	
Independent Claims	1 - 3 =	-0-	x $78.00	$	
Multiple Dependent Claim(s) (if applicable)			+ $260.00	$	
TOTAL OF ABOVE CALCULATIONS =				$ 970.00	
Reduction by 1/2 for filing by **small entity**, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$ 970.00	
Processing fee of $130 for furnishing the **English translation** later than ☐ **20** ☐ **30** months from the earliest claimed priority date (37 CFR 1.492(f))				$	
TOTAL NATIONAL FEE =				$ 970.00	
Fee of $40.00 for recording the enclosed **assignment** (37 CFR 1.21(h)). Assignment must be accompanied by appropriate cover sheet (37 CFR 3.28, 3.31).				$	
TOTAL FEES ENCLOSED =				$ 970.00	
				Amt. to be refunded:	$
				Amt. charged:	$

a. ☒ A check in the amount of $ 970.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. **06-1358** in the amount of $ --- to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge my account any additional fees set forth in §1.492 during the pendency of this application, or credit any overpayment to Deposit Account No. **06-1358**. A duplicate copy of this sheet is enclosed.

SEND ALL CORRESPONDENCE TO:
Jacobson, Price, Holman & Stern, PLLC
400 7th Street, N.W., Suite 600
Washington, DC 20004
202-638-6666
CUSTOMER NUMBER: 00136

By _____
John C. Holman
Reg. No. 22,769

JPH&S 3/95

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Kevin DEWAR et al.

Serial No.: New

Filed: June 15, 2000

For: AN ATM CELL PROCESSOR

PRELIMINARY AMENDMENT TO LESSEN FEES

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE CLAIMS

Claim 3, line 1, delete "claims 1 or 2",
insert --claim 1--;

Claim 4, line 1, delete "any preceding claim",
insert --claim 1--;

Claim 5, line 1, delete "claims 3 or 4",
insert --claim 3--;

Claim 6, line 1, delete "claims 4 or 5",
insert --claim 4--;

Claim 7, line 1, delete "any preceding claim",
insert --claim 1--;

Claim 9, line 1, delete "any preceding claim",
insert --claim 1--;

Claim 10, line 1, delete "any preceding claim",
insert --claim 1--;

Claim 12, line 1, delete "any preceding claim",
insert --claim 1--;

Claim 13, line 1, delete "any preceding claim",
insert --claim 1--;

Claim 17, line 1, delete "or 16",

Claim 18, line 1, delete "any preceding claim",
insert --claim 1--.

Applicant: Kevin DEWAR et al.

REMARKS

The foregoing Preliminary Amendment is requested in order to delete the multiple dependent claims and avoid paying the multiple dependent claims fee.

Early action on the merits is respectfully requested.

Respectfully submitted,

JACOBSON, PRICE, HOLMAN & STERN, PLLC

By _____
John C. Holman
Reg. No. 22,769

400 Seventh Street, N.W.
Washington, D.C. 20004-2201
(202) 638-6666

Date: June 15, 2000
Atty. Docket: P65633US0
JCH/cmf

"An ATM Cell Processor"

INTRODUCTION

Field of the Invention

The invention relates to a processor for handling asynchronous transfer mode (ATM) cells.

Prior Art Discussion

The ATM technique supports many different services such as voice, frame relay, or circuit emulation. Also, the throughput rates are quite high, in the order of hundreds of thousands of cells per second.

The general approach has been to provide extensive circuitry to handle the many cell processing functions required. For example, European Patent Specification No. EP614324 (Nippon) describes circuitry having cell assembly and disassembly control circuits and memory access control circuits.

Such circuits tend to be limited in their functionality and to be complex.

Objects of the Invention

An object of the invention is to provide for efficient handling of cells by a processor. Another object is that the processor has flexibility in the manner in which it operates so that it may be used in different environments with relatively simple configuration.

A still further object is to provide a cell processor which may be controlled in a comprehensive manner with relatively simple control circuits.

SUMMARY OF THE INVENTION

According to the invention, there is provided an ATM cell processor comprising a line interface, a backplane interface, and processing means for identifying cells according to their headers and processing the identified cells.

Thus the processor may be integrated in a flexible manner in a system having multiple cell streams.

In one embodiment, the line and backplane interfaces are bi-directional. This provides excellent versatility for cell processing.

In one embodiment, the processing means comprises a mapping function. This allows mapping of received cells according to the VPI/VCI.

Preferably, the mapping function comprises means for changing the cell headers according to mapped cell destinations.

In one embodiment, the mapping function comprises means for adding an additional header to a cell for internal control signalling.

In another embodiment, the processing means further comprises a policing function for monitoring traffic characteristics. This allows integration in a system connected to multiple client systems and is particularly useful for monitoring contracts.

In a further embodiment, the processing means comprises a queueing function connected between the interfaces for controlling transfer of cells to the line interface. This provides for effective cell traffic management.

In another embodiment, the queueing function comprises means for interfacing with a cell memory for storage of cell queues, and with a control memory for storing queueing

parameter values. This enhances flexibility in the manner in which cells are queued. It also provides for simple queueing control.

In one embodiment, the queueing function is connected to a memory controller for interfacing with the cell and control memories.

Preferably, the queueing function comprises means for managing path descriptor tables in the control memory.

In another embodiment, the queueing function comprises means for managing queue descriptor tables, each relating to individual queues in the control memory.

In one embodiment, the cell processor further comprises a segmentation and reassembly (SAR) interface for routing of cells to an external SAR device. This allows connection of the cell processor to a control processor in an efficient manner using cells for control signalling.

Preferably, the SAR interface is connected to the queueing function.

In one embodiment, the cell processor comprises a control processor interface for connection to a memory controller to allow initial set-up configuration.

DETAILED DESCRIPTION OF THE INVENTION

Brief Description of the Drawings

The invention will be more clearly understood from the following description of some embodiments thereof, given by way of example only with reference to the accompanying drawings in which:-

Fig. 1 is a schematic representation of a cell processor of the invention;

Fig. 2 is a diagram illustrating operation of a queue server matrix; and

Fig. 3 is a diagram illustrating a UTOPIA interface of the cell processor.

Description of Embodiments

Referring to Fig. 1, there is shown a cell processor 10 of the invention. The processor 10 is an application specific integrated circuit (ASIC), the application being processing of ATM cells.

The main components of the ASIC 10 are now briefly described briefly with reference to general signal flows through the processor. The cell rate handled is 373 K cells per second, which represents a bit rate of greater than 155 Mpps. The ASIC 10 has a backplane interface 11 for interfacing according to the CUBIT™ protocol via a backplane.

A queueing function 12 performs extensive buffering operations using DRAM or SRAM external to the ASIC 10 and is accessed via a CellRAM controller 13. It also uses an SRAM controller 14 for access to additional off-chip SRAM. The off-chip memory is used in general for such things as manipulating link lists, and storing cells awaiting transfer. More specifically, the SRAM accessed by the SRAM controller 14 is used effectively as an external register and to store queue parameters including the queue sizes. On the other hand, the DRAM or SRAM accessed via the CellRAM controller 13 is used for storing actual cells. When dequeueing from the Cell RAM, the SRAM is used to track the cells using pointer information.

Cells received in the direction A at the backplane interface 11 are passed to the queueing function 12, and may be routed to CellRAM. Continuing on the path A indicated in Fig. 1, the cells are then transferred to a multi-PHY line interface 15. This is a master

interface which supports many ports, in this embodiment eight. Again, the UTOPIA protocol is used.

Thus, in the path A, the ASIC 10 does not change the cells, but does manage output to the line by using queueing mechanisms and external memory.

In the opposite direction, cells are received as indicated by the arrow B at the line interface 15 and are transferred to a mapping function 16. The mapping function 16 changes the VCI/VPI headers according to the destination of the cells and by doing this, it re-directs them to the correct destination. It does not "know" what the different cell streams represent, but it identifies the streams by their headers. The cells are passed to a policing function 17 which operates according to algorithms to evaluate certain policing parameters such as the cell rate for a particular contract. Various parameters are taken into account such as the temporary nature of any usage of excessive bandwidth for a particular contract. The SRAM accessed via the SRAM controller 14 is used for some of these functions. After the policing functions, the cells are transferred to the backplane interface 11.

The ASIC 10 also comprises a processor interface 20 and a configuration and status function 21, which are connected to the queueing function 12 and the SRAM controller 14. This allows a microprocessor to access the ASIC 10 and perform a limited set of functions including initial setup and configuration and subsequent status monitoring. An important initial setup function is configuration of the SRAM 14. Subsequently, the processor can access the SRAM locations via the controller 14 and the interface 20 to monitor parameters such as the count of dropped cells.

An important aspect of the ASIC 10 is that it can use control signals communicated in the ATM format. To do this, it uses a segmentation and reassembly (SAR) interface 25 which is connected to a SAR device which performs AAL5 segmentation and reassembly of ATM messages. This interface is used for communication of ATM messages with a SAR device. The SAR device interfaces with another device such as a microprocessor

(possibly the same microprocessor as is connected to the interface 20) for comprehensive control communication. The ATM nature of the communication is transparent to the microprocessor because of operation of the SAR device. Thus, a single microprocessor may have access to the ASIC 10 in two different manners, one being a direct access for initial setup and monitoring of parameters, the other being for comprehensive control communication.

Referring again to the direction A of Fig. 1 the cells which are received at the backplane interface 11 are queued in one of the multiple queues depending on their VPI/VCI. The queues are serviced on a pre-programmed basis to implement a priority queueing system. Queues that grow too large may have cells discarded on a configured basis. Statistics are kept on the number of cells received, the number of cells transmitted, the number of bad cells, and the number of cells dropped due to congestion.

Queueing is initialised by a microprocessor using the configuration and status function 21. This function has registers, in which there is a notional split of registers related to queueing and those related to dequeueing. The queueing function 12 uses a significant number of tables to control the buffering and congestion management functions. One such table is a path descriptor, the start address of which is provided by a configuration register. The VPI of an incoming cell is used to form an offset into this table. In addition there are special path descriptors for mapping, for the SAR, and for the processor, the addresses again being provided by configuration registers.

Another table is a queue descriptor, which contains information about an individual queue. All queues are identical, however, they may appear to have different priorities depending on programming of a queue server matrix. Queues are irrevocably tied to target output ports and each of the eight line ports has eight queues associated with it. In addition, a single queue is maintained for each of the processor, SAR, and mapping entities. Mapping between queues and targets is specified in two tables, one for each of aggregate and tributary modes. Each queue has a four-word descriptor, and the offset

from the value of the configuration register holding the start location is simply the queue number multiplied by four.

A queue server matrix 30 is shown in Fig. 2. It controls the order in which queues are serviced. Its location and maximum size (1024 elements) are indicated by configuration registers. Each element (31) of the matrix holds eleven used fields. Each field is associated with a queue. The queues are checked in ascending order, i.e. the first queue checked is the most significant byte of the first word. Within each byte, only the least significant seven bits are meaningful, i.e. bits 6 to 0. The value in a field indicates the priority level for the associated queue.

Storage pools of the queues are referred to as heaps, and consist of stacks of DRAM addresses. There are twenty heaps maintained. The heap structure is implemented as a set of pointers kept internally and also the DRAM addresses which are stored in the SRAM. Initialisation of the heap involves programming up the pointers into SRAM for the top-of-stack and start-of-stack for each used heap, and then initialisation of the SRAM location between those two pointer values with a unique and valid set of DRAM locations. Configuration registers are used for programming the heap pointers.

These features provide excellent flexibility in the manner in which queues are set up and dynamically managed.

As shown in Fig. 1, the output cells of the queueing function are transferred to the line interface 15 or the SAR interface 25.

In the opposite direction, cells received at the line interface 15 are passed to the mapping and policing functions 16 and 17. The cells are passed to the backplane interface 11, to the queueing function 12, or are dropped. Again, the configuration registers store the initialisation information. SRAM tables are maintained by the functions 16 and 17. There are five tables associated with the mapping function 16 as follows:

- per port statistics table,
- VCC connection table,
- dequeue connection table, and
- secondary mapping descriptor table.

Storage of these tables is set by the configuration registers. The per port statistics table stores information including the numbers of cells with invalid and disabled VPI/VCIs and with unsupported PTIs. It also includes the VPI/VCIs of the last disabled and invalid cells.

The VCC connection table contains the following information on a per connection basis:-

mapping descriptor,

received cell count,

dropped cell count, and

GCRA words 1 – 4.

The VPC connection table is identical, except that VPIs are used in place of VCIs.

The dequeue connection table has a maximum of 1024 entries and consists of 1024 32 bit mapping descriptors.

The secondary mapping descriptor table consists of 4096 32 bit entries. Each secondary mapping descriptor is 14 bits long, as set out below.

Field Name	Size	Bit Position
Reserved	18	14-31
map_vpi	1	13
cell_routing	3	10-12
vci_map	10	0-9

Referring now to the three UTOPIA interfaces 11, 15, and 25, Fig. 3 shows an overview. All of the interfaces use the appropriate Start-of-Cell (SOC) signal to initialise cell reception from an external source. Each interface counts octets and an error indication is given when a SOC is activated at an unexpected time. This gives a warning of malformed cells entering the ASIC whilst providing a mechanism to recover at the next cell boundary. Short cells are discarded, whilst long cells are truncated and passed on. Both cause an error indication. Before cells are transferred internally, they are synchronised to the internal common system clock "sys clk". A phase locked loop (PLL) 40 provides the internal clock signal from an external microprocessor 42. A SAR device 43 is shown connected to the SAR interface 25. Also, line and backplane devices 44 and 45 are shown connected to their respective interfaces.

It will be appreciated that the invention provides for very efficient processing of ATM cells between a line and a backplane. Varying rates of cell transfer are handled effectively by the queueing mechanism. The circuit also supports many different services by efficiently routing cell streams. The circuit also allows policing functions to be implemented very efficiently with little effect on cell transfer rates.

The invention is not limited to the embodiments described, but may be varied in construction and detail within the scope of the claims.

Amended Claims

1. An ATM cell processor comprising a line interface, a backplane interface, and a processing means between the interfaces for processing cells according to their headers, characterised in that:-

the processing means comprises a segmentation and reassembly (SAR) interface (25);

the processing means comprises a queueing function (12) comprising means for controlling transfer of cells to the line interface (15) and to the SAR interface (25) according to the cell headers; and

the processing means further comprises a mapping function (16) comprising means for changing cell headers during transfer from the line interface (15) to the backplane interface (11) according to mapped cell destinations.

2. An ATM cell processor as claimed in claim 1, wherein the queueing function (12) comprises means for receiving control cells from the SAR interface (25).

3. An ATM cell processor as claimed in claims 1 or 2, wherein the processing means further comprises a cell memory controller (13) for interfacing with an external cell memory, and the queueing function (12) comprises means for accessing a cell memory via said controller (13).

4. An ATM cell processor as claimed in any preceding claim, wherein the processing means further comprises a control memory controller (14) for interfacing with an external control memory, and the queueing function (12) comprises means for accessing a control memory via said controller (14).

5. An ATM cell processor as claimed in claims 3 or 4, wherein the queueing function (12) comprises means for dequeueing from a cell memory and for tracking the cells using pointer information retrieved from a control memory.

6. An ATM cell processor as claimed in claims 4 or 5, wherein the processing means further comprises a configuration and status function (21) connected to the queueing function (12) and to the control memory controller (14), and means (20) for allowing an external microprocessor access said control memory for initial setup and configuration and subsequent status monitoring.

7. An ATM cell processor as claimed in any preceding claim, wherein the queueing function (12) comprises means for managing path descriptor tables (30) in a control memory.

8. An ATM cell processor as claimed in claim 7, wherein the queueing function comprises means for using the VPI of an incoming cell to form an offset into the path descriptor table.

9. An ATM cell processor as claimed in any preceding claim, wherein the queueing function (12) comprises means for managing queue description tables, each relating to individual queues, in the control memory.

10. An ATM cell processor as claimed in any preceding claim, wherein the queueing function (12) comprises means for managing a queue server matrix, the location and size of which is indicated by configuration registers, and in which each element of the matrix stores a plurality of fields and each field is associated with a queue.

11. An ATM cell processor as claimed in claim 10, wherein the queueing function (12) comprises means for checking queues in ascending order in an element by starting with a most significant byte in the fields of each element.

12. An ATM cell processor as claimed in any preceding claim, wherein the queueing function (12) comprises means for maintaining a plurality of queue storage pool heaps by maintaining a set of pointers programmed using configuration registers.

13. An ATM cell processor as claimed in any preceding claim, wherein the mapping function (16) comprises means for adding an additional header to a cell for internal control signalling.

14. An ATM cell processor as claimed in claim 13, wherein the mapping function (16) comprises means for passing cells to the queueing function (12), for passing cells to the backplane interface (11), and for dropping cells.

15. An ATM cell processor as claimed in claim 14, wherein the mapping function (16) comprises means for maintaining tables in a control memory.

16. An ATM cell processor as claimed in claim 15, wherein the tables comprise a per port statistics table storing data indicating the numbers of cells with invalid and disabled VPI/VCIs and with unsupported PTIs.

17. An ATM cell processor as claimed in claim 15 or 16, wherein the tables comprise a VCC connection table containing the following information on a per connection basis:-

mapping descriptor,

received cell count,

dropped cell count, and

GCRA words.

18. An ATM cell processor as claimed in any preceding claim, wherein the processing means further comprises a policing function (17) comprising means for monitoring traffic characteristics.

19. An ATM cell processor as claimed in claim 18, wherein the policing function (17) is connected between the mapping function (16) and the backplane (11) and comprises means for monitoring traffic characteristics of cell streams outputted by the mapping function (16) to the backplane interface (11).

Abstract

An ATM cell processor (10) has a backplane interface (11), a line interface (15), and various processing functions between the interfaces. Cells directed to the line interface (15) are controlled by a queueing function (12) which uses external cell memory via a controller (13) and external control memory via a controller (14). Cells from the backplane are identified and routed by a mapping function (16).

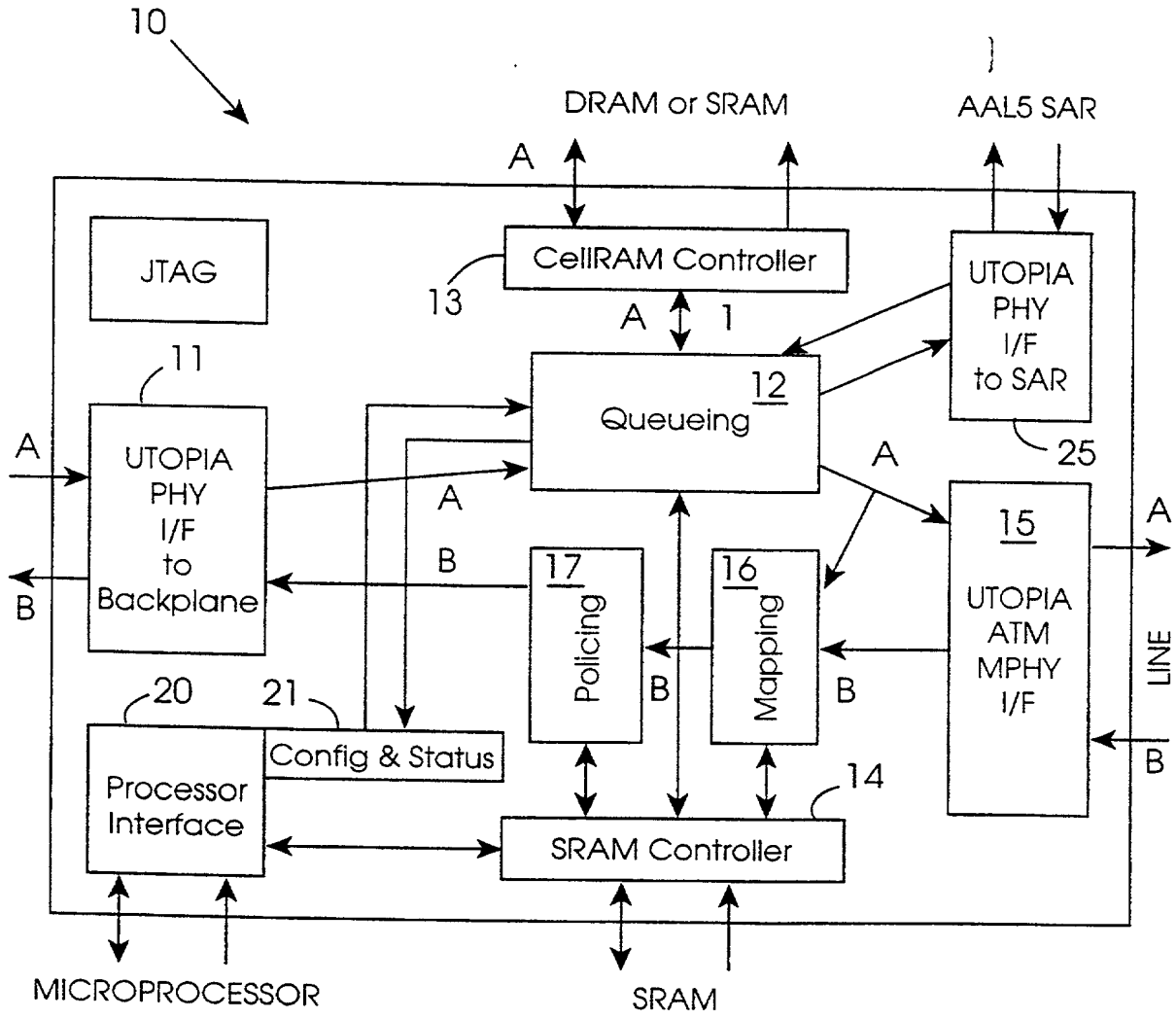
10
DRAM or SRAM
AAL5 SAR
A
JTAG
CellRAM Controller
13
A
1
UTOPIA
PHY
I/F
to SAR
11
12
Queueing
25
A
UTOPIA
PHY
I/F
to
Backplane
A
B
B
17
Policing
16
Mapping
15
UTOPIA
ATM
MPHY
I/F
A
LINE
B
B
B
20
21
Config & Status
Processor
Interface
14
SRAM Controller
MICROPROCESSOR
SRAM

Fig. 1

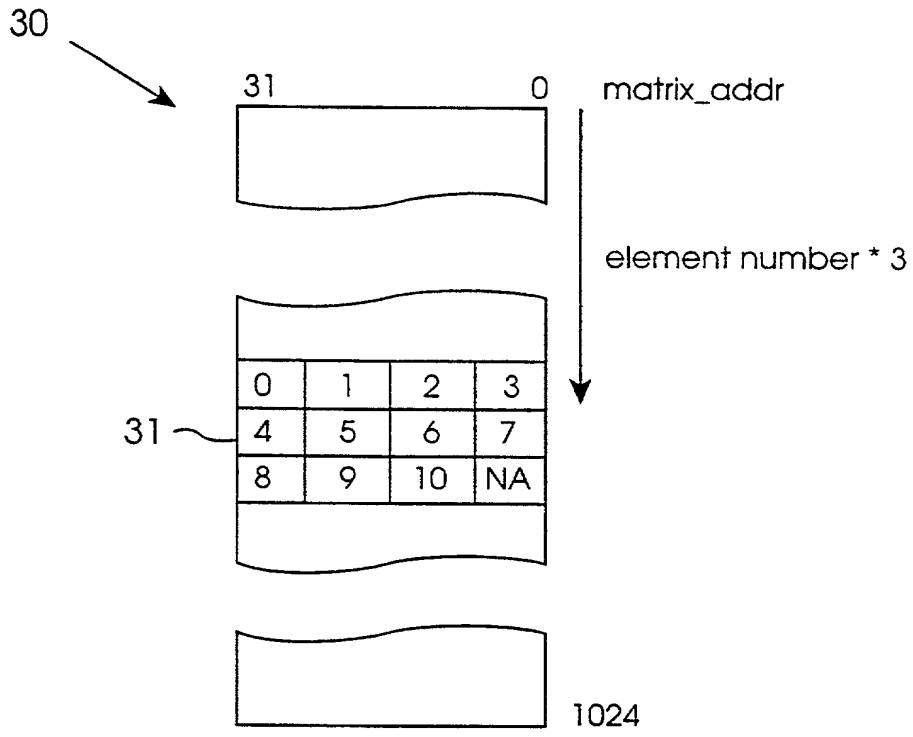

Fig. 2

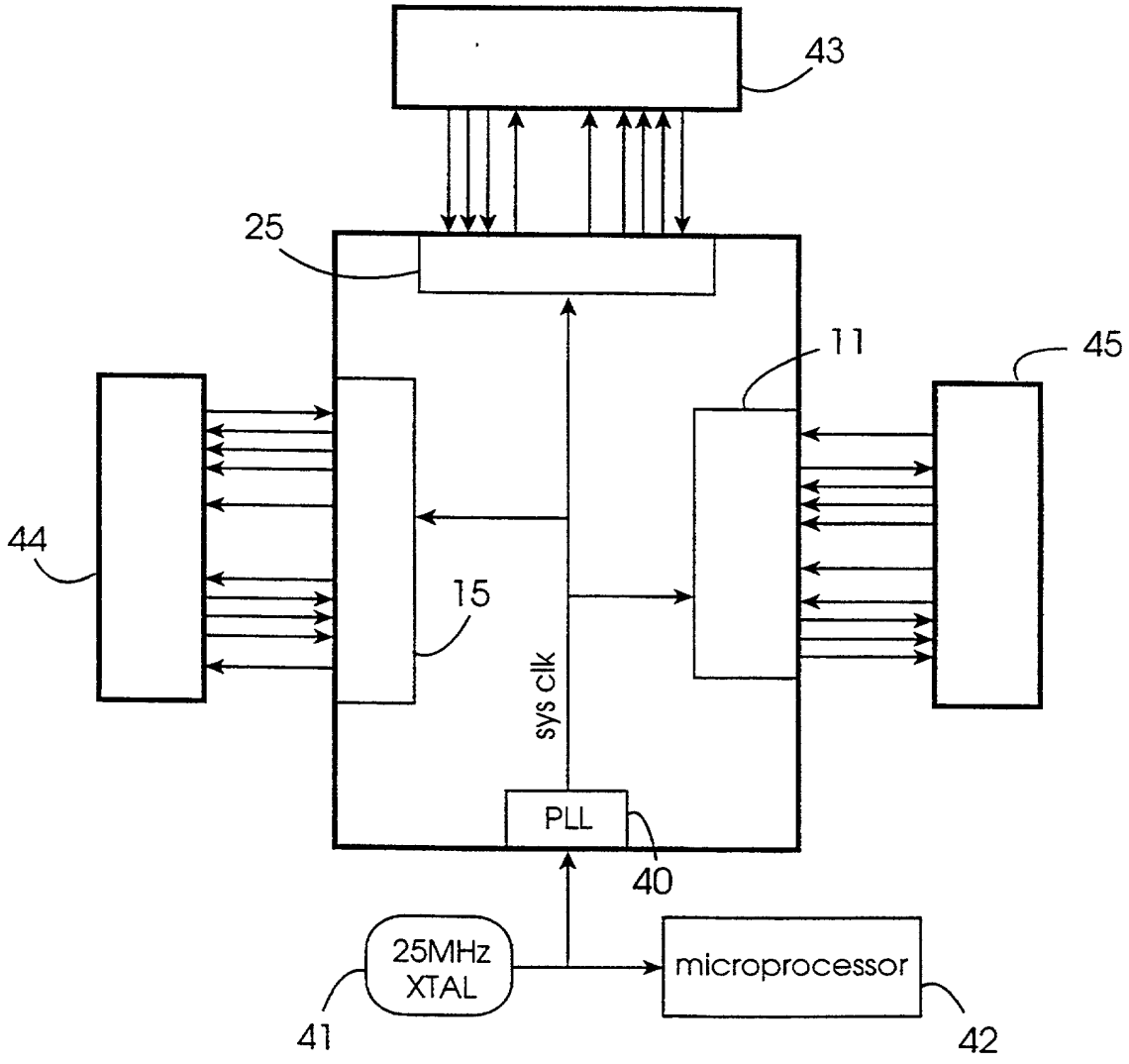
43
25
11
45
44
15
sys clk
PLL
40
25MHz
XTAL
microprocessor
41
42

Fig. 3

ALL PATENTS, INCLUDING DESIGN
FOR APPLICATION BASED ON PCT; PARIS CONVENTION;
NON PRIORITY; OR PROVISIONAL APPLICATIONS

DECLARATION AND POWER OF ATTORNEY U.S.A.

FOR ATTORNEY'S USE ONLY

ATTORNEY'S DOCKET NO.

As a below named inventor, I declare that my residence, post office address and citizenship are stated below next to my name, the information given herein is true, that I believe that I am the original, first and sole inventor (if only one name is listed at 201 below), or a first and joint inventor (if plural inventors are named below at 201-203, or an additional sheets attached hereto) of the subject matter which is claimed and for which patent is sought on the invention entitled:

101 **An ATM Cell Processor**

102 which is described and claimed in: [X] PCT International Application No. PCT/IE98/00106 filed ____

[ ] the attached specification [ ] the specification in application Serial No. ____ filed ____ (if applicable) and amended on ____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.
I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

103

Prior Foreign Application(s) (Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed Yes	No
970888	IE	15/12/1997	X	
S980712	IE	31/08/1998	X	

104 I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

Application No. ____ Filing Date ____ Application No. ____ Filing Date ____

105 I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of the application:

(Application Serial No.) ____ (Filing Date) ____ (Status: patented, pending, abandoned) ____

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys (Registration No.) to prosecute this application, receive and act on instructions from my agent, and transact all business in the Patent and Trademark Office connected therewith. HARVEY B. JACOBSON JR. (20,851); D. DOUGLAS PRICE (24,514); JOHN CLARKE HOLMAN (22,769); MARVIN R. STERN (20,640); MICHAEL R. SLOBASKY (26,421); JONATHAN L. SCHERER (29,851); IRWIN M. AISENBERG (19,007); WILLIAM E. PLAYER (31,409)

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO: (please use Attorney's Docket No.) (202) 638-6666
JACOBSON, PRICE, HOLMAN & STERN PROFESSIONAL LIMITED LIABILITY COMPANY 400 SEVENTH STREET N.W. WASHINGTON, DC. 20004	JACOBSON, PRICE, HOLMAN & STERN PROFESSIONAL LIMITED LIABILITY COMPANY

*Inventor(s) name must include at least one unabbreviated first or middle name.

201	FULL NAME OF INVENTOR *	FAMILY NAME O'Dowd	GIVEN NAME Brendan		MIDDLE NAME	
	RESIDENCE & CITIZENSHIP	CITY Limerick	STATE OR FOREIGN COUNTRY Ireland		COUNTRY OF CITIZENSHIP Ireland	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS 4 Ashmount, Raheen	CITY Limerick	STATE OR COUNTRY Ireland		ZIP CODE
202	FULL NAME OF INVENTOR *	FAMILY NAME Dewar	GIVEN NAME Kevin		MIDDLE NAME	
	RESIDENCE & CITIZENSHIP	CITY Clare	STATE OR FOREIGN COUNTRY County Clare		COUNTRY OF CITIZENSHIP Ireland	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS Stone Park, Ballyallia, Ennis	CITY County Clare	STATE OR COUNTRY Ireland		ZIP CODE
203	FULL NAME OF INVENTOR *	FAMILY NAME Brebner	GIVEN NAME Gavin		MIDDLE NAME	
	RESIDENCE & CITIZENSHIP	CITY Emilly	STATE OR FOREIGN COUNTRY France		COUNTRY OF CITIZENSHIP Great Britain	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS 73 Chemin Charriere Blache	CITY Emilly	STATE OR COUNTRY France		ZIP CODE 69130

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201 *	SIGNATURE OF INVENTOR 202 *	SIGNATURE OF INVENTOR 203 *
X [signature]		
DATE X 6/12/00	DATE	DATE

* Additional inventors are named on separately numbered sheets attached hereto.

ALL PATENTS, INCLUDING DESIGN
FOR APPLICATION BASED ON PCT; PARIS CONVENTION;
NON PRIORITY; OR PROVISIONAL APPLICATIONS

DECLARATION AND POWER OF ATTORNEY U.S.A.

FOR ATTORNEY'S USE ONLY

ATTORNEY'S DOCKET NO.

#1

As a below named inventor, I declare that my residence, post office address and citizenship are stated below next to my name, the information given herein is true, that I believe that I am the original, first and sole inventor (if only one name is stated at 201 below), or a first and joint inventor (if plural inventors are named below at 201-203, or on additional sheets attached hereto) of the subject matter which is claimed and for which patent is sought on the invention entitled:

101 **An ATM Cell Processor**

102 which is described and claimed in: [X] PCT International Application No. PCT/IE98/00106 filed ____

[ ] the attached specification [ ] the specification in application Serial No. ____ filed ____

(if applicable) and amended on ____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.
I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

103

Prior Foreign Application(s) (Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed Yes	No
970888	IE	15/12/1997	X	
S980712	IE	31/08/1998	X	

104 I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date	Application No.	Filing Date

105 I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys (Registration No.) to prosecute this application, receive and act on instructions from my agent, and transact all business in the Patent and Trademark Office connected therewith. HARVEY B. JACOBSON JR. (20,851); D. DOUGLAS PRICE (24,514); JOHN CLARKE HOLMAN (22,769); MARVIN R. STERN (20,640); MICHAEL R. SLOBASKY (26,421); JONATHAN L. SCHERER (29,851); IRWIN M. AISENBERG (19,007); WILLIAM E. PLAYER (31,409)

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
JACOBSON, PRICE, HOLMAN & STERN PROFESSIONAL LIMITED LIABILITY COMPANY 400 SEVENTH STREET N.W. WASHINGTON, DC. 20004	(please use Attorney's Docket No.) (202) 638-6666 JACOBSON, PRICE, HOLMAN & STERN PROFESSIONAL LIMITED LIABILITY COMPANY

*Inventor(s) name must include at least one unabbreviated first or middle name.

201	FULL NAME OF INVENTOR *	FAMILY NAME: Dewar	GIVEN NAME: Kevin	MIDDLE NAME:	
	RESIDENCE & CITIZENSHIP	CITY: Clare	STATE OR FOREIGN COUNTRY: Ireland IEX	COUNTRY OF CITIZENSHIP: Ireland	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS: Stone Park, Ballyallia, Ennis	CITY: County Clare	STATE OR COUNTRY: Ireland	ZIP CODE:
202	FULL NAME OF INVENTOR *	FAMILY NAME: O'Dowd	GIVEN NAME: Brendan	MIDDLE NAME:	
	RESIDENCE & CITIZENSHIP	CITY: Limerick	STATE OR FOREIGN COUNTRY: Ireland IEX	COUNTRY OF CITIZENSHIP: Ireland	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS: 4 Ashmount, Raheen	CITY: Limerick	STATE OR COUNTRY: Ireland	ZIP CODE:
203	FULL NAME OF INVENTOR *	FAMILY NAME: Brebner	GIVEN NAME: Gavin	MIDDLE NAME:	
	RESIDENCE & CITIZENSHIP	CITY: Emilly	STATE OR FOREIGN COUNTRY: France FRX	COUNTRY OF CITIZENSHIP: Great Britain	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS: 73 Chemin Charriere Blache	CITY: Emilly	STATE OR COUNTRY: France	ZIP CODE: 69130

I further declare that all statements made herein of my own knowledge are true and that all statement made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201 *	SIGNATURE OF INVENTOR 202 *	SIGNATURE OF INVENTOR 203 *
X Kevin Dewar	X	X
DATE X 2nd June 2000	DATE X	DATE X 14/12/2000

* Additional inventors are named on separately numbered sheets attached hereto. JPH&S 1995 8/95; 3/96; 5/98 (COPYING WITHOUT DELETIONS PERMITTED)